1.Feature

ROM: 2K x 14 bits
RAM: 72 x 8 bits
STACK: 2 Levels
Advance mode and General mode
I/O ports: 20 I/O PAD
Timer/counter: 8bits x1 (TMR0)
Prescaler: 3 Bits
Watchdog Timer: On chip WDT based on internal RC oscillator. The shortest period is 21mS; user can extend the WDT overflow period to 2.688S by using prescaler.
Power-On Reset & Watchdog timer overflow Reset & Low Voltage reset.
Reset Timer: 21 mS (5V)
Four external Oscillate modes: RC,LP Crystal,NT Crystal and HS Crystal.
Operation Voltage: 2.2V～5.5V
Instruction set: 78
Wake-up: Port B pin-change wake-up (Advanced mode only).
Pull-UP : Port B input pull-up (Advanced mode only).
Reset vector: 7FFH

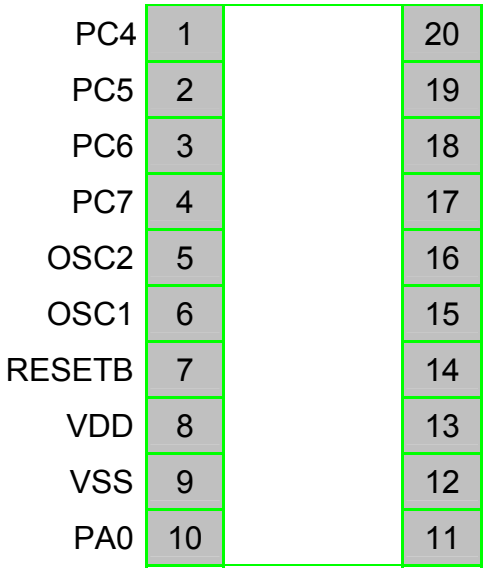
2. Pin Definition & Pad Assignment

EXT_CLK/PA4	1		28	RESETB
VDD	2		27	OSC1
NC	3		26	OSC2
VSS	4		25	PC7
NC	5		24	PC6
PA0	6		23	PC5
PA1	7		22	PC4
PA2	8		21	PC3
PA3	9		20	PC2
PB0	10		19	PC1
PB1	11		18	PC0
PB2	12		17	PB7
PB3	13		16	PB6
PB4	14		15	PB5

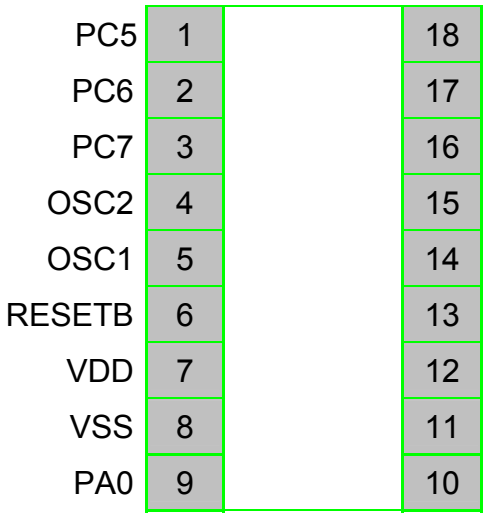
Package Types :SDIP(TM58PC20ASD28C)、
DIP(TM58PC20AD28C)、
SOP(TM58PC20AS28C)

VSS	1		28	RESETB
EXT_CLK/PA4	2		27	OSC1
VDD	3		26	OSC2
VDD	4		25	PC7
PA0	5		24	PC6
PA1	6		23	PC5
PA2	7		22	PC4
PA3	8		21	PC3
PB0	9		20	PC2
PB1	10		19	PC1
PB2	11		18	PC0
PB3	12		17	PB7
PB4	13		16	PB6
VSS	14		15	PB5

Package Types :SSOP(TM58PC20ASS28C)



Package Types :SDIP(TM58PC20ASD20C)、
SOP(TM58PC20AS20C)



Package Types :SDIP(TM58PC20ASD18C)、
SOP(TM58PC20AS18C)

PIN description

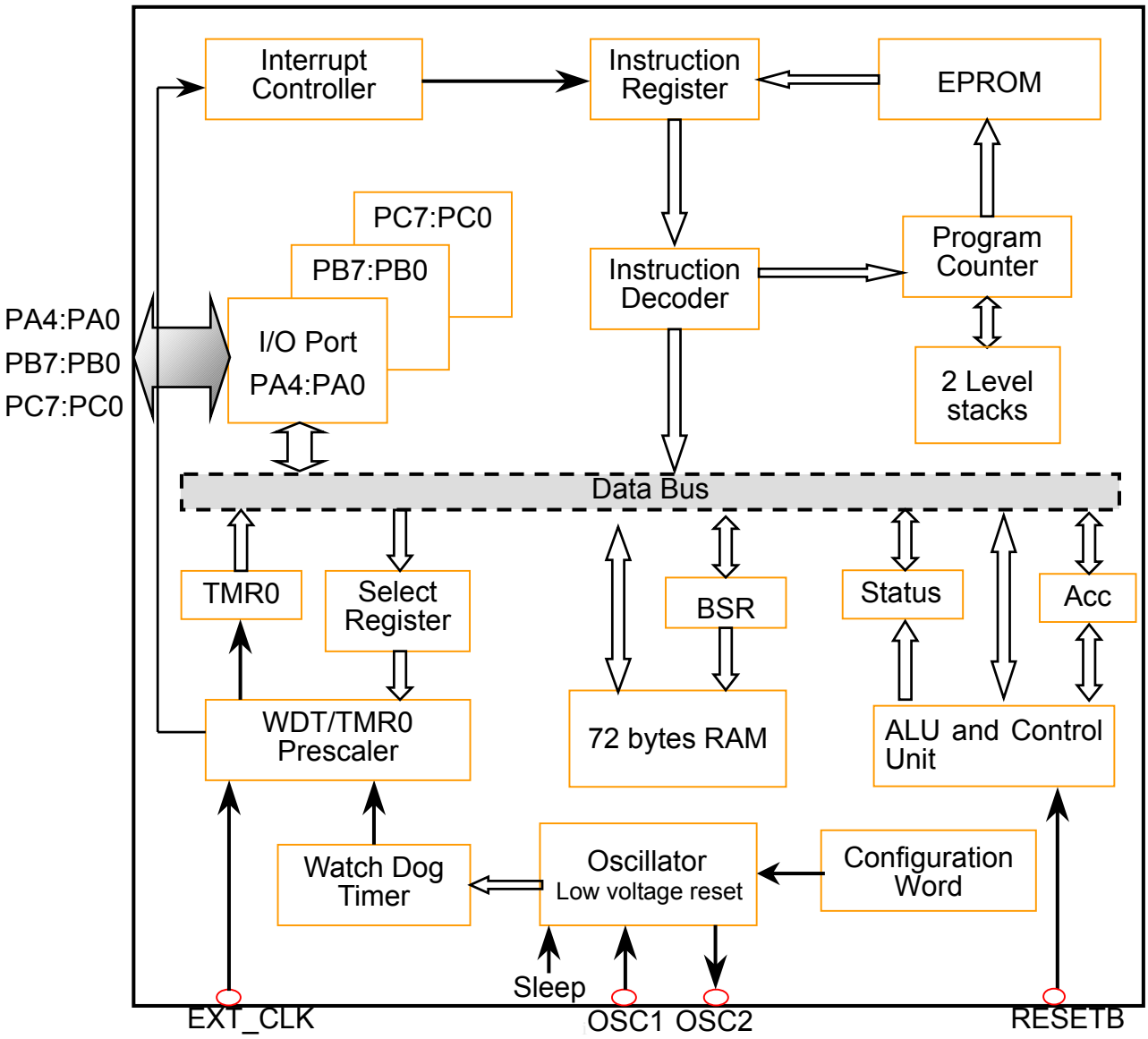
Pin name	I/O	Description
EXT_CLK/ PA4	I	1. External clock input to TMR0 counter 2. PA4 input (When config bit7=1, Advance mode only)
PA3-0	I/O	I/O port
PB7-0	I/O	1. I/O port 2. Pin-change wake-up (Advanced mode only) 3. Pull-UP (Advanced mode only)
PC7-0	I/O	I/O port
RESETB	I	System reset signal input
OSC1	I	Oscillator input
OSC2	O	Oscillator output
VDD	P	Power input
VSS	P	Ground input

I: Input; O: Output; I/O: Bi-direction; P: Power

3. Control Register

Name	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG (Instruction)		RTCEN	TYPE	LV1	LV0	CPT	WDTE	FOSC1	FOSC0
SELECT				SUR0	EDGE0	PSA	PS2	PS1	PS0
IAR	$00		A6	A5	A4	A3	A2	A1	A0
TMR0	$01	D7	D6	D5	D4	D3	D2	D1	D0
PC	$02	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	$03		SA1	SA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
BSR	$04		D6	D5	D4	D3	D2	D1	D0
I/O PortA	$05				PA4	PA3	PA2	PA1	PA0
I/O PortB	$06	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
I/O PortC	$07	PC7	PC6	PB5	PC4	PC3	PC2	PC1	PC0

4. System Block Diagram



5. Memory Map

TM58PC20A memory is organized into program memory and data memory.

5.1 Program memory

There are only 512 words of the same page that can be directly addressed. Extra program memory can be addressed by setting bit 6~5 of status register. The sequence of instructions is controlled via the program counter (PC), which automatically increases 1. However, the sequence can be changed by skip, call and goto instructions or by moving data to the PC.

TM58PC20A has an 11-bits program counter capable of accessing 2K spaces. If accessing address has over 2K, then the address will map to physical 2K memories, i.e. 2K+M will be mapped to M. A NOP at the reset vector location will cause a restart at address 000h. A simple map to induce illustrate ROM organization is shown in figures 5-1.

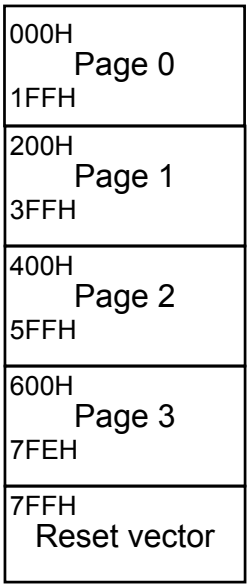


Figure 5-1 The ROM Organization

5.2 Configuration memory

The configuration word is located 800H that contains OSC selection, WDT enable, code protection and type selection.

Bit	Symbol	Description			
1~0	FOSC1~FOSC0	Bit_1	Bit_0	OSC Type	Resonance Frequency
		0	0	LP (low speed)	32~200K Hz
		0	1	NT(Normal speed)	200K~10M Hz
		1	0	HS (high speed)	10~20M Hz
		1	1	RC	32K ~ 10 M Hz
2	WDTE	WDTE: Watchdog enable/disable control 1: WDT enable 0: WDT disable			
3	CPT	CPT: Code Protection bit 1: OFF 0: ON			
5~4	LV1~LV0	LV1	LV0	Detect voltage	
		0	0	4.0V	
		0	1	Don't use	
		1	0	2.3V	
		1	1	Don't use	
6	TYPE	TYPE: Select operating mode 1: Advanced mode (PB pin-change wakeup & PB pull-up enable) 0: General mode			
7	RTCEN	1		PA4 input	
		0		Timer input only	

Figure 5-2 The Configuration Word

5.3 Data memory

Data memory is composed of special function registers and general-purpose ram. TM58PC20A has 72 general-purpose registers that accessed by using a bank select scheme. The special function registers include the program counter (PC), the timer (TMR0) register, the status register, the bank select register, and the I/O port registers. Furthermore, TM58PC20A has 3 auxiliary registers that include indirect addressing register (IAR), the select register (Select) and the I/O direction register (IODIR). The register map of TM58PC20A is shown in figure 5-3.

<table>
<tr><th></th><th>Bank0</th><th>Bank1</th><th>Bank2</th><th>Bank3</th></tr>
<tr><td>00h</td><td>IAR</td><td colspan="3" rowspan="8">Map back to address in Bank0</td></tr>
<tr><td>01h</td><td>TMR0</td></tr>
<tr><td>02h</td><td>PC</td></tr>
<tr><td>03h</td><td>STATUS</td></tr>
<tr><td>04h</td><td>BSR</td></tr>
<tr><td>05h</td><td>PORTA</td></tr>
<tr><td>06h</td><td>PORTB</td></tr>
<tr><td>07h</td><td>PORTC</td></tr>
<tr><td>08h~0FH</td><td>General Purpose Register</td><td colspan="3"></td></tr>
<tr><td>8+16*4=72</td><td>General Purpose Register
10-1F</td><td>General Purpose Register
30-3F</td><td>General Purpose Register
50-5F</td><td>General Purpose Register
70-7F</td></tr>
</table>

Figure 5-3 The Register Map of TM58PC20A

A. The IAR (indirect addressing register) is not a physical register and is used to assist BSR with indirect addressing. Any instruction attempts to access IAR actually mapping to another address that is pointed by BSR. Since IAR is not a material circuit, user reads IAR itself (BSR=00H) will always return 00h at data bus. Writing to IAR itself will like NOP.

B. Select register is used to control WDT and TMR0. It has not assigned a specific address in data memory and can only set control bits by select instruction, i.e. it is write-only register. The context of accumulator will be sent to the select register by executing the select instruction. If select register has never set by program, its default value is 3FH. We drew Figure 5-4 to explain how to set select register.

Bit	Symbol	Description				
		PS2	PS1	PS0	TMR0 rate	WDT rate
2~0	PS2~PS0	0	0	0	1:2	1:1
		0	0	1	1:4	1:2
		0	1	0	1:8	1:4
		0	1	1	1:16	1:8
		1	0	0	1:32	1:16
		1	0	1	1:64	1:32
		1	1	0	1:128	1:64
		1	1	1	1:256	1:128
3	PSA	PSA: Prescaler assignment bit 1: Prescaler assigned to WDT 0: Prescaler assigned to TMR0				
4	EDGE0	EDGE0: TMR0 source signal edge control bit 1:increment when H→L transition on external clock 0:increment when L→H transition on external clock				
5	SUR0	SUR0: TMR0 clock source bit 1: EXT_CLK input 0: (System clock)/4 or internal instruction cycle				

Figure 5-4 Select Register

C. The I/O Direction control register is similar to the Select register that is write-only register. To set an I/O port pin as input, the corresponding direction control bit must be high. Similarly, the zero represents output. Any direction control bit can be programmed individually as input or output by using IODIR instruction. If the register is not programmed, than all I/O ports always keep input mode.

- PC (program counter) is 11-bit wide binary counter and increases itself for every instruction cycle, except the following conditions.
  1. call, goto, lgoto and lcall: the label will move to PC
  2. retla and ret: the top value of stack will pop to PC

  Incrementing PC when it changes to the next higher page. It should be noted that the page select bits in the status register would not be changed synchronously. The following Goto, Call, or MOVAM 02H will return to the previous page, unless the page select bits have been updated in program. In order to reduce the complexity of programming, TM58PC20A provides 2 instructions to facilitate subroutine call and branch handling which are LCALL and LGOTO. LCALL and LGOTO can address to anywhere in the ROM, but the page select bits are unnecessary. The attached operands of CALL and GOTO are 8-bit and 9-bit respectively, and so need extra bits (page select bits) to address whole memory. However, LCALL and LGOTO have 11-bit wide operands that are easy to address the total ROM space.

- TMR0 is 8-bit wide binary counter/timer. This register increases by an external signal edge applied to EXT_CLK pin, or by internal instruction cycle. It has the following features.

  A. Readable and writeable
  B. Synchronize with 2 internal clocks
  C. Can use programmable prescaler by setting select register

  The other details will be described in follow-up chapter.

- Status register contains page select bits, time out bit, power down bit and the status of ALU. Please note that $\overline{TO}$ and $\overline{PD}$ are controlled by hardware and unchangeable by program.

<table>
<tr><th>Bit</th><th>Symbol</th><th colspan="3">Description</th></tr>
<tr><td rowspan="3">0</td><td rowspan="3">C</td><td colspan="3">Carry and $\overline{Borrow}$ bit:</td></tr>
<tr><td colspan="2">ADD instruction</td><td>SUB instruction</td></tr>
<tr><td colspan="2">1: a carry occurred from the MSB
0: no carry</td><td>1: no borrow (Note1)
0: a borrow occurred from the MSB</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">DC</td><td colspan="3">Nibble Carry and Nibble $\overline{Borrow}$ bit</td></tr>
<tr><td colspan="2">ADD instruction</td><td>SUB instruction</td></tr>
<tr><td colspan="2">1: a carry from the low nibble bits of the result occurred
0: no carry</td><td>1: no borrow
0: a borrow from the low nibble bits of the result occurred</td></tr>
<tr><td>2</td><td>Z</td><td colspan="3">Zero bit:
1: the result of a logic operation is zero
0: the result of a logic operation is not zero</td></tr>
<tr><td>3</td><td>$\overline{PD}$</td><td colspan="3">Power down flag bit: (Note2)
1: after power-on or by the CLRWDT instruction
0: execute SLEEP instruction</td></tr>
<tr><td>4</td><td>$\overline{TO}$</td><td colspan="3">Time out flag bit:
1: after power-on or by the CLRWDT or SLEEP instruction
0: Occur WDT time-overflow</td></tr>
<tr><td rowspan="5">6~5</td><td rowspan="5">SA1~SA0</td><td>SA1</td><td>SA0</td><td>Page Location</td></tr>
<tr><td>0</td><td>0</td><td>Page 0 (000H~1FFH)</td></tr>
<tr><td>0</td><td>1</td><td>Page 1 (200H~3FFH)</td></tr>
<tr><td>1</td><td>0</td><td>Page 2 (400H~5FFH)</td></tr>
<tr><td>1</td><td>1</td><td>Page 3 (600H~7FFH)</td></tr>
</table>

Figure 5-5 Status Register

Note1: A SUB instruction is executed by adding the 2's complement of the subtrahend, so C = 1 represents positive result. The Figure 5-5-1 show the relation between C-bit and borrow.

B0H－50H										50H－B0H									
	C	B7	B6	B5	B4	B3	B2	B1	B0		C	B7	B6	B5	B4	B3	B2	B1	B0
＋ ＝	1	1 1 0	0 0 1	1 1 1	1 1 0	0 0 0	0 0 0	0 0 0	0 0 0	＋ ＝	0	0 0 1	1 1 0	0 0 1	1 1 0	0 0 0	0 0 0	0 0 0	0 0 0

Figure 5-5-1

Note2: The $\overline{TO}$ and $\overline{PD}$ bits are active low that can be used to determine different causes of reset. The Figure 5-5-2 illustrates the value of $\overline{TO}$ and $\overline{PD}$ after the relative reset events.

$\overline{TO}$	$\overline{PD}$	Reset Event
0	0	WDT time out from sleep mode
0	1	WDT time out from normal mode
1	0	RESETB reset from sleep
1	1	Power on reset
Unchanged	Unchanged	RESETB reset from normal

Figure 5-5-2

- BSR (bank select register) is associated with IAR to indirectly access the data memory. The direct addressing must rely on BSR to access bank1 ~ bank3, because there are only 5-bit wide address operands in general mode. The bit 6~5 of BSR are used to select the specifiable memory bank. These address regions 20H~2FH, 40H~4FH and 60H~6FH are not accessible, these address will be mapped to 00H~0FH (Bank0). The addressing map is shown in Figure 5-6.

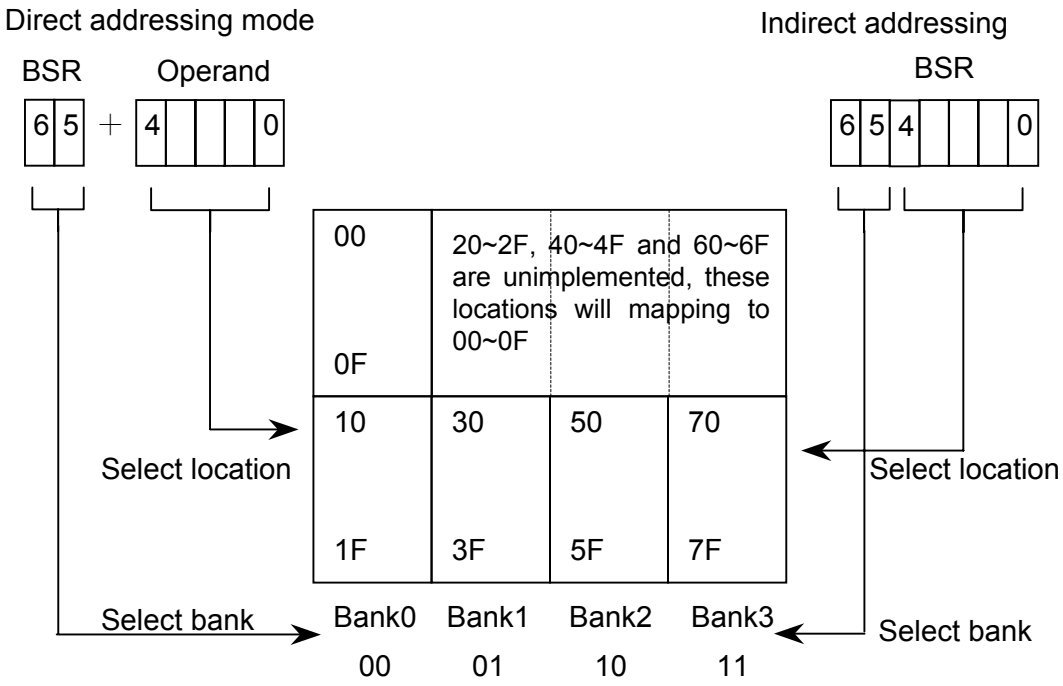


Figure 5-6 The Direct and Indirect Addressing Map

- Port A~C are programmable I/O ports. Please note that read I/O instruction always read the I/O pin even though the pin is output mode. On reset, all I/O pins were set as input mode until IODIR has been changed.

6. Functional Description

6.1 TMR0 and Watchdog timer

Fig. 6-1 shows the block diagram of the TMR0/WDT prescaler. As shown in the figure, the prescaler register can be a pre-scaler for TMR0 or be a post-scaler for WDT.

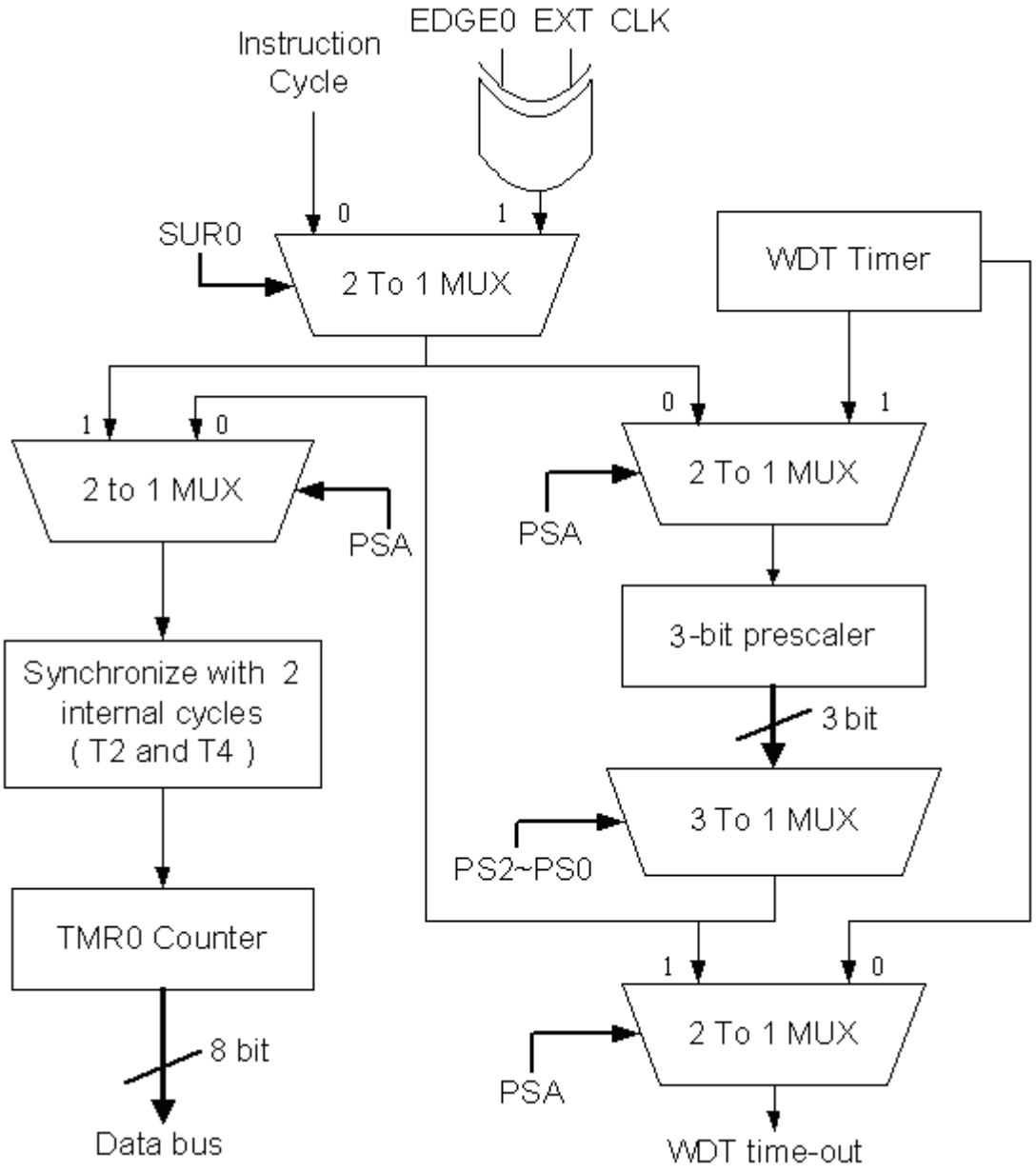


Figure 6-1 Block Diagram of the TMR0/WDT Prescaler

The TMR0 is an 8-bit timer/counter. The clock source of TMR0 can come from the instruction clock or the external clock.

A. To select the instruction clock, the SUR0 bit of the select register should be clear. When no prescaler is used, TMR0 will increase by 1 at every instruction cycle.
B. To select the external clock, the SUR0 bit of the select register should be set. In this mode, TMR0 relies on the EDGE0 bit to determine that TMR0 is increased by 1 at every falling or rising edge. When an external clock is used for TMR0, a problem must be noted that the external clock synchronizes with internal clock. TM58PC20A synchronizes external clock by sampling internal clock at T2 and T4. If external pulse is smaller than 2 internal cycles, the pulse maybe ignored. Therefore, the external clock must keep stable state (high or low) for at least 2 internal cycles.

The WDT counter is an 8-bit binary counter. The clock source of WDT is provided by an independent on-chip RC oscillator that does not need any external clock. Therefore, the WDT will keep counting even if the chip has slept already. A WDT time-overflow will restart system and set the time-overflow flag bit (bit4 of status register) as " 0 ". The WDT time-overflow period vary with temperature, power voltage and process. This period can be improved via the prescaler. The maximum division ratio can up to 1:128 by setting PS2~PS0 as "111".

The prescaler can be assigned to either the TMR0 or the WDT via the PSA bit. Note that either WDT or TMR0 can employ the prescaler simultaneously. The following Example(2-3) must be executed when changing PSA form TMR0 to the WDT and form WDT to the TMR0 respectively. These examples can avoid an unintended time-overflow reset.

```
Clrwdt
Clrm      TMR0;  clear prescaler & TMR0
Movla     B'00xx1111'
Select
Clrwdt
Movla     B'00xx1xxx';set prescaler to
desired
```

Example 2 Changing prescaler form TMR0

```
Clrwdt   ; clear prescaler & WDT
Movla       B'00xx0xxx'
Select   ; set prescaler to TMR0
with
         ; new rate
```

Example 3 Changing prescaler form WDT to TMR0

When the prescaler is assigned to WDT, “CLRWDT” and “SLEEP” instruction will clear the prescaler and the WDT. When the prescaler is assigned to TMR0, the prescaler will be cleared by any instruction that writes to TMR0.

6.2 Reset

TM58PC20A may be reset by one of the following conditions:

(1) Power-on

(2) RESETB pin input a negative pulse

(3) WDT timer out reset (if enabled).

(4) Low Voltage reset

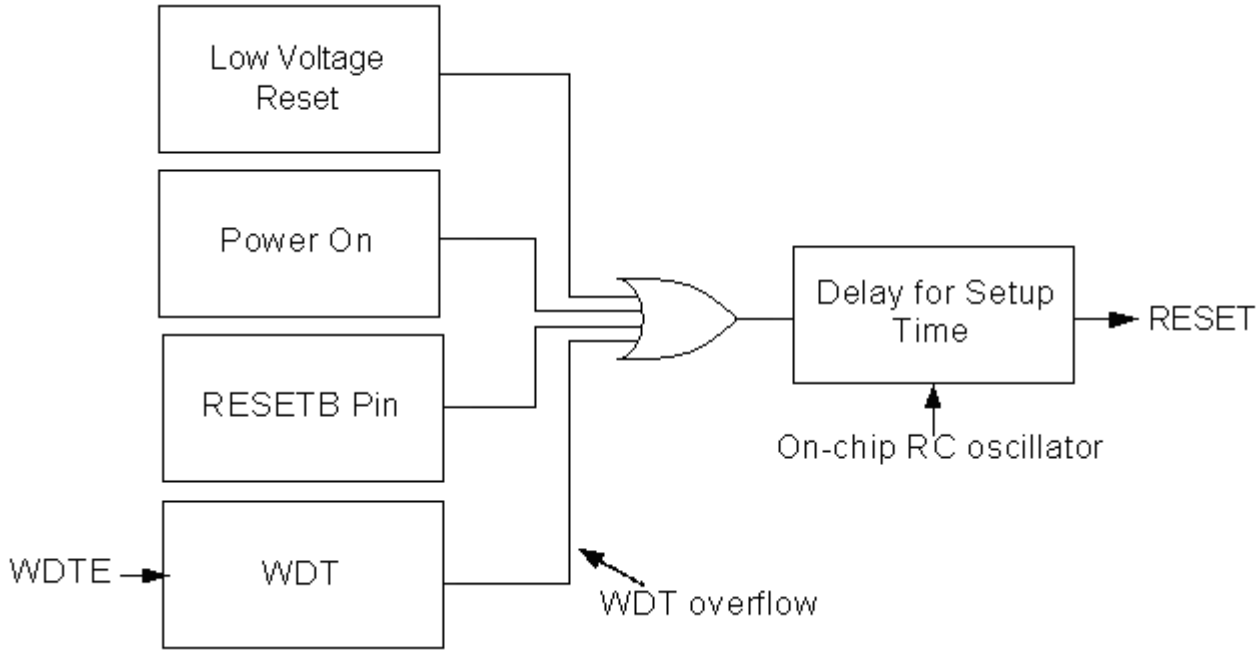


Figure 6-2 Scheme of the Reset Controller

As shown in the figure 6-2, three reset conditions are listed. In general, we call the first one reset-cases as cold reset. The cold reset time may be too short for slow crystals and RC oscillators that require much longer than setup time (note) to oscillate.

Note: the setup time is approximately 21ms that will affect due to power voltage, process and temperature variations.

The last two cases are called warm reset. The different reset events will affect registers and ram. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the type of reset. These relation are listed in figure 6-3

Address	Name	Cold Reset	Warm Reset
N/A	Accumulator	xxxx xxxx	pppp pppp
N/A	IODIR	1111 1111	1111 1111
N/A	Select	--11 1111	--11 1111
00h	IAR	---- ----	---- ----
01h	TMR0	xxxx xxxx	pppp pppp
02h	PC	111 1111 1111	111 1111 1111
03h	STATUS	0001 1xxx	000? ?ppp [1]
04h	BSR	1xxx xxxx	1ppp pppp
05h	PORTA	000x xxxx	000p pppp
06h	PORTB	xxxx xxxx	pppp pppp
07h	PORTC	xxxx xxxx	pppp pppp
	General Purpose RAM	xxxx xxxx	pppp pppp

6-3 RESET CONDITIONS

X: unknown; P: previous data ; ?: value depends on condition ;

6.3 ADVANCED MODE

In advanced mode , we provide wake up function. Chip can be wake up from Sleep mode when the logic of the input pin of the PortB is changed. So we need to read the logic of the input pin before sleep. In advanced mode, the use of a pull-up resistor for the input pin of PortB. You can set the I/O direction of PortB by “IODIR” instruction . If the chip wake up from sleep state, the next instruction of SLEEP will be executed.

Wake up

```
movla       0fh
iodir       06h;; set i/o direction of portb
  .          .
movm        06h,a ;; read the voltage of the input pin before sleep
sleep            ;; only portb3210 cab be wakeup
call        delay26ms ;;this instruction will be executed after wake up
```

Example 1 : Wake up

The debounce time is the interval that must pass before a second pressing of a key is accepted. User can set this interval with the delay routine (See Example 1).

Key bounce

```
After_wakeup
;-------------------------------------
int_nt1                ;; filter out key begin bounce
   btmsc   06h,0
   lgoto   int_nt1
int_loop1               ;; filter out key end bounce
   call    delay        ;; worse case 30ms
   btmss   06h,0
   lgoto   int_loop1

   call    delay_routine    ;; such as 30ms
   btmss   06h,0
   lgoto   int_loop1
;-------------------------------------
```

Example 2 : Key_Debounce

7. Instruction Set

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	OP-code
ADDAM M, m	(M)+(acc) → (M)	1	C, DC, Z	10 0101 1MMM MMMM
ADDAM M, a	(M)+(acc) → (acc)	1	C, DC, Z	10 0101 0MMM MMMM
ANDAM M, m	(M) · (acc) → (M)	1	Z	10 0100 1MMM MMMM
ANDAM M, a	(M) · (acc) → (acc)	1	Z	10 0100 0MMM MMMM
ANDLA I	Literal · (acc) → (acc)	1	Z	11 1001 iiii iiii
BCM M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BCM M, b1	Clear bit1 of (M)	1	None	00 1100 1MMM MMMM
BCM M, b2	Clear bit2 of (M)	1	None	00 1101 0MMM MMMM
BCM M, b3	Clear bit3 of (M)	1	None	00 1101 1MMM MMMM
BCM M, b4	Clear bit4 of (M)	1	None	00 1110 0MMM MMMM
BCM M, b5	Clear bit5 of (M)	1	None	00 1110 1MMM MMMM
BCM M, b6	Clear bit6 of (M)	1	None	00 1111 0MMM MMMM
BCM M, b7	Clear bit7 of (M)	1	None	00 1111 1MMM MMMM
BSM M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BSM M, b1	Set bit1 of (M)	1	None	00 1000 1MMM MMMM
BSM M, b2	Set bit2 of (M)	1	None	00 1001 0MMM MMMM
BSM M, b3	Set bit3 of (M)	1	None	00 1001 1MMM MMMM
BSM M, b4	Set bit4 of (M)	1	None	00 1010 0MMM MMMM
BSM M, b5	Set bit5 of (M)	1	None	00 1010 1MMM MMMM
BSM M, b6	Set bit6 of (M)	1	None	00 1011 0MMM MMMM
BSM M, b7	Set bit7 of (M)	1	None	00 1011 1MMM MMMM
BTMSC M, b0	If bit0 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTMSC M, b1	If bit1 of (M) = 0, skip next instruction	1 + (skip)	None	00 0100 1MMM MMMM
BTMSC M, b2	If bit2 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 0MMM MMMM
BTMSC M, b3	If bit3 of (M) = 0, skip next instruction	1 + (skip)	None	00 0101 1MMM MMMM
BTMSC M, b4	If bit4 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 0MMM MMMM
BTMSC M, b5	If bit5 of (M) = 0, skip next instruction	1 + (skip)	None	00 0110 1MMM MMMM
BTMSC M, b6	If bit6 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 0MMM MMMM

BTMSC M, b7	If bit7 of (M) = 0, skip next instruction	1 + (skip)	None	00 0111 1MMM MMMM
BTMSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTMSS M, b1	If bit1 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 1MMM MMMM
BTMSS M, b2	If bit2 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 0MMM MMMM
BTMSS M, b3	If bit3 of (M) = 1, skip next instruction	1 + (skip)	None	00 0001 1MMM MMMM
BTMSS M, b4	If bit4 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 0MMM MMMM
BTMSS M, b5	If bit5 of (M) = 1, skip next instruction	1 + (skip)	None	00 0010 1MMM MMMM
BTMSS M, b6	If bit6 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 0MMM MMMM
BTMSS M, b7	If bit7 of (M) = 1, skip next instruction	1 + (skip)	None	00 0011 1MMM MMMM
CALL I	Call subroutine	2	None	11 0110 iiii iiii
CLRA	Clear accumulator	1	Z	10 0001 0000 0000
CLRM M	Clear memory M	1	Z	10 0001 1MMM MMMM
CLRWDT	Clear watch-dog register	1	TO, PO	10 0000 0000 0001
COMM M, m	~(M) → (M)	1	Z	10 0010 1MMM MMMM
COMM M, a	~(M) → (acc)	1	Z	10 0010 0MMM MMMM
DECM M, m	Decrement M to M	1	Z	10 0110 1MMM MMMM
DECM M, a	(M) - 1 → (acc)	1	Z	10 0110 0MMM MMMM
DECMSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	10 0111 1MMM MMMM
DECMSZ M, a	(M) - 1 → (acc), skip if (M) = 0	1 + (skip)	None	10 0111 0MMM MMMM
GOTO I	Goto branch	2	None	11 101i iiii iiii
INCM M, m	(M) + 1 → (M)	1	Z	10 1000 1MMM MMMM
INCM M, a	(M) + 1 → (acc)	1	Z	10 1000 0MMM MMMM
INCMSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 + (skip)	None	10 1001 1MMM MMMM
INCMSZ M, a	(M) + 1 → (acc), skip if (M) = 0	1 + (skip)	None	10 1001 0MMM MMMM
IODIR M	Set i/o direction	1	None	10 0000 0000 0MMM
IORAM M, m	(M) ior (acc) → (M)	1	Z	10 1111 1MMM MMMM
IORAM M, a	(M) ior (acc) → (acc)	1	Z	10 1111 0MMM MMMM
IORLA I	Literal ior (acc) → (acc)	1	Z	11 0011 iiii iiii

LCALL I	Call subroutine. However, LCALL can addressing 2K address	2	None	01 0iii iiii iiii
LGOTO I	Go branch to any address	2	None	01 1iii iiii iiii
MOVAM m	Move data form acc to memory	1	None	10 0000 1MMM MMMM
MOVLA I	Move literal to accumulator	1	None	11 0001 iiii iiii
MOVM M, m	(M) → (M)	1	Z	10 0011 1MMM MMMM
MOVM M, a	(M) → (acc)	1	Z	10 0011 0MMM MMMM
NOP	No operation	1	None	10 0000 0000 0000
RET	Return	2	None	11 1111 0111 1111
RETLA I	Return and move literal to accumulator	2	None	11 1100 iiii iiii
RLM M, m	Rotate left from m to itself	1	C	10 1100 1MMM MMMM
RLM M, a	Rotate left from m to acc	1	C	10 1100 0MMM MMMM
RRM M, m	Rotate right from m to itself	1	C	10 1110 1MMM MMMM
RRM M, a	Rotate right from m to acc	1	C	10 1110 0MMM MMMM
SELECT	Set select register	1	None	10 0000 0000 0010
SLEEP	Enter sleep (saving) mode	1	TO, PO	10 0000 0000 0011
SUBAM M, m	(M)–(acc) → (M)	1	C, DC, Z	10 1010 1MMM MMMM
SUBAM M, a	(M) – (acc) → (acc)	1	C, DC, Z	10 1010 0MMM MMMM
SWAPM M, m	Swap data from m to itself	1	None	10 1101 1MMM MMMM
SWAPM M, a	Swap data from m to acc	1	None	10 1101 0MMM MMMM
XORAM M, m	(M) xor (acc) → (M)	1	Z	10 1011 1MMM MMMM
XORAM M, a	(M) xor (acc) → (acc)	1	Z	10 1011 0MMM MMMM
XORLA I	Literal xor (acc) → (acc)	1	Z	11 1000 iiii iiii

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Supply Voltage …. Vss-0.3V to Vss+5.5V　Storge Temperature …….–50℃ to 125℃
Input Voltage …… Vss-0.3V to VDD+0.3V　Operating Temperature…　0℃ to 70℃

8.2 DC Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	---		2.2		5.5	V
V_{DVT}	Detect Voltage	5V	Low Voltage reset (Idd = 3uA) Config bit6.bit5=00		4.0		V
		3V	Low Voltage reset (Idd = 1.5uA) Config bit6.bit5=10		2.3		V
		5V	I/O Port	2		VDD	V
V_{IL}	Input Low Voltage	5V	I/O Port			0.8	V
I_{DD1}	Standby Current	5V	LVD disable,WDT disable, LV disable		1		uA
			LVD disable,WDT enable, LV disable		7		
		3V	LVD disable,WDT disable, LV disable		1		
			LVD disable,WDT enable, LV disable		1.5		
I_{IL}	Input Leakage Current	5V	Vin=VDD, VSS		1		uA
		3V	Vin=VDD, VSS		1		
I_{OH}	I/O Port Driving Current	5V	Voh=4.5V		9		mA
			Voh=4V		13		
			Voh=3.5V		22		
		3V	Voh=2.7V		3.3		
			Voh=2.1V		7		
			Voh=1.5V		10.4		
I_{OL}	I/O Port Sink Current	5V	Vol=0.5V		21		mA
			Vol=01V		37		
			Vol=1.5V		49		
		3V	Vol=0.3V		10		
			Vol=0.9V		20		
			Vol=1.5V		24		
R_{PUHI}	Pull up resistance	5V	PortB input only		160		KΩ
		3V	PortB input only		310		

8.3 AC Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
		VDD	Conditions				
f_{sys1}	System Clock	5V	LP Crystal mode	32		200	Khz
		3V		32		200	
f_{sys1}	System Clock	5V	NT Crystal mode	0.2		10	Mhz
		3V		0.2		10	
f_{sys3}	System Clock	5V	HS Crystal mode	10		20	Mhz
		3V					
f_{sys4}	System Clock	5V	RC mode			10	Mhz
		3V				10	
T_{wdt}	Watchdog Timer	5V			21		mS
		3V			26		
T_{rht}	Reset Hold Time	5V			21		mS
		3V			26		

8.4 External RC Tables

RC 頻率表(5V, 25℃), Sample S1~S6

R	C	S1	S2	S3	S4	S5	S6	Freq(unit)
7.5M	0.1u	6.757	6.25	6.757	6.944	6.707	6.706	K Hz
	20p	6.667	6.25	6.849	7.143	6.858	6.901	
	--(1)	6.944	7.353	6.757	7.143	7.012	7.201	
6M	0.1u	8.605	7.463	8.197	8.772	8.233	8.132	
	20p	8.333	7.692	8.197	8.929	8.707	8.700	
	--	8.475	8.621	8.065	8.772	8.485	8.880	
330K	0.1u	95.04	93.46	99.01	102.0	96.40	95.12	
	20p	99.01	93.46	99.01	103.1	96.44	95.32	
	--	100	100	99.96	101.0	100.2	100.6	
300K	0.1u	104.2	108.7	105.3	104.2	105.2	103.1	
	20p	105.1	108.9	105.3	104.6	104.2	106.6	
	--	106.4	105.3	109.9	109.9	108.3	108.0	
150K	0.1u	207.3	204.1	212.8	200	205.1	203.4	
	20p	208.3	204.1	212.8	200	208.0	206.2	
	--	212.8	208.3	222.2	217.7	215.6	215.4	
120K	0.1u	255.1	250	257.7	263.2	257.8	258.3	
	20p	257.7	247.5	257.7	266.0	260.2	261.2	
	--	270.3	270.3	277.8	277.8	271.3	274.6	
75K	0.1u	427.4	420.4	420.2	420.2	400	421.2	
	20p	413.2	419	431.0	420.2	403.1	421.2	
	--	454.5	454.6	438.6	439.6	446.1	447.2	
68K	0.1u	463	463	463	463	463	462.8	
	20p	463	463	463	463	463	463	
	--	500	500	501	490.2	499.9	498.5	
39K	0.1u	819.7	806.5	819.7	833.3	822.3	825.3	
	20p	847.5	826.4	840.3	854.7	840.2	841.6	
	--	877.2	877.2	888.3	892.9	879.2	879.5	
36K	0.1u	892.9	892.9	909.1	925.9	910.3	912.6	
	20p	925.9	925.9	925.9	943.4	925.9	923.6	
	--	925.9	925.9	925.9	926.5	925.3	924.9	

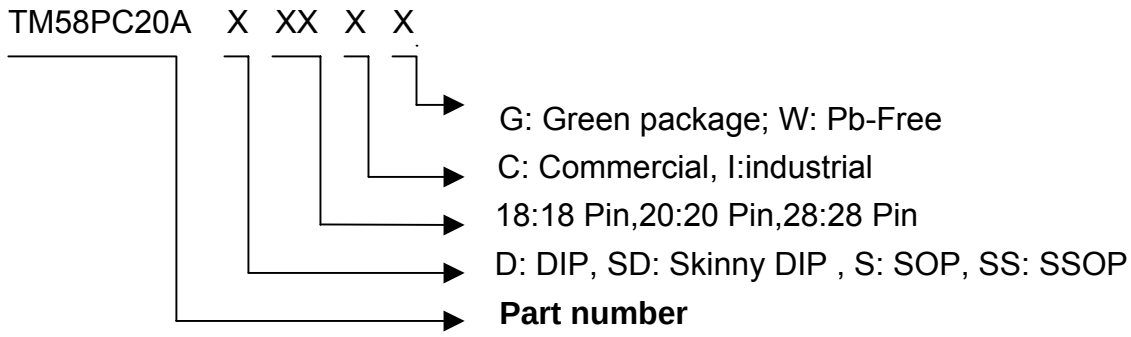
VDD = 5V

R	C	S1	S2	S3	S4	S5	S6	Freq(unit)
20K	0.1u	1.724	1.695	1.695	1.695	1.696	1.680	M Hz
	20p	1.754	1.786	1.754	1.786	1.754	1.756	
	--	1.754	1.768	1.754	1.755	1.757	1.749	
18K	0.1u	1.838	1.868	1.838	1.825	1.838	1.849	
	20p	1.838	1.880	1.825	1.852	1.827	1.852	
	--	1.923	1.887	1.852	1.856	1.889	1.880	
15K	0.1u	2.294	2.252	2.252	2.294	2.278	2.279	
	20p	2.315	2.315	2.294	2.305	2.306	2.310	
	--	2.358	2.358	2.404	2.427	2.419	2.506	
12K	0.1u	2.857	2.778	2.778	2.778	2.779	2.780	
	20p	2.941	2.941	2.941	2.875	2.942	2.941	
	--	3.030	3.001	2.941	2.948	2.990	2.967	
10K	0.1u	3.571	3.571	3.571	3.571	3.571	3.572	
	20p	3.571	3.571	3.571	3.571	3.570	3.573	
	--	3.676	3.371	3.676	3.623	3.684	3.668	
9.1K	0.1u	3.968	3.968	3.906	3.968	3.969	3.960	
	20p	3.968	4.032	3.968	3.968	3.967	3.969	
	--	4.032	3.968	3.968	3.970	3.971	3.973	
8.2K	0.1u	4.545	4.545	4.545	4.545	4.544	4.543	
	20p	4.348	4.545	4.545	4.545	4.546	4.547	
	--	4.629	4.630	4.630	4.808	4.630	4.631	
7.5K	0.1u	5.051	5	4.95	5.051	5.000	5.010	
	20p	5.051	5	5.102	5.012	5.107	5.016	
	--	4.902	4.091	5.000	4.909	4.903	4.905	
5.6K	0.1u	6.757	6.757	6.757	6.754	6.752	6.755	
	20p	6.944	6.944	6.944	7.143	6.950	6.955	
	--	6.757	6.757	6.759	6.754	6.755	6.757	

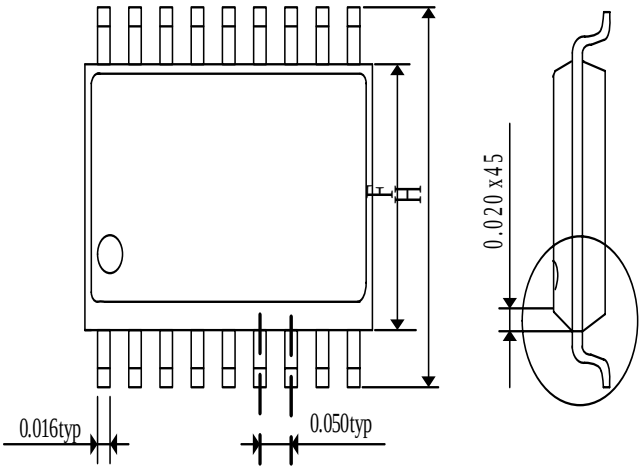
Note 1 : No capacitor.

Note 2 : This frequency is unstable.

9. Part number Guide



18 PIN SOP

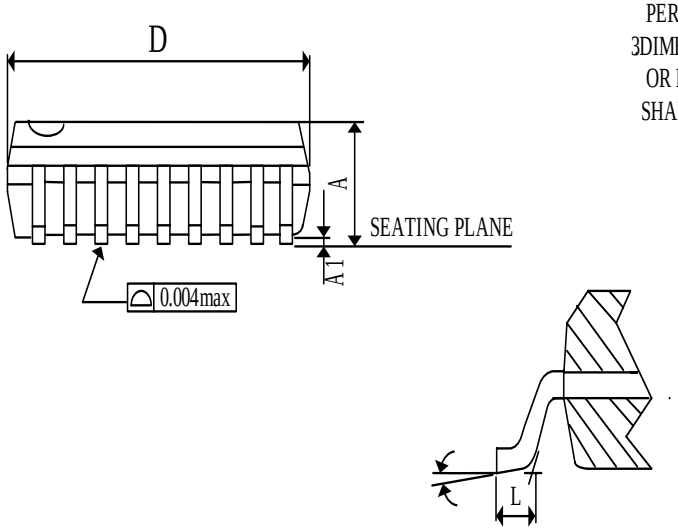


Symbol	MIN	MAX
A	0.093	0.104
A1	0.004	0.012
D	0.447	0.463
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

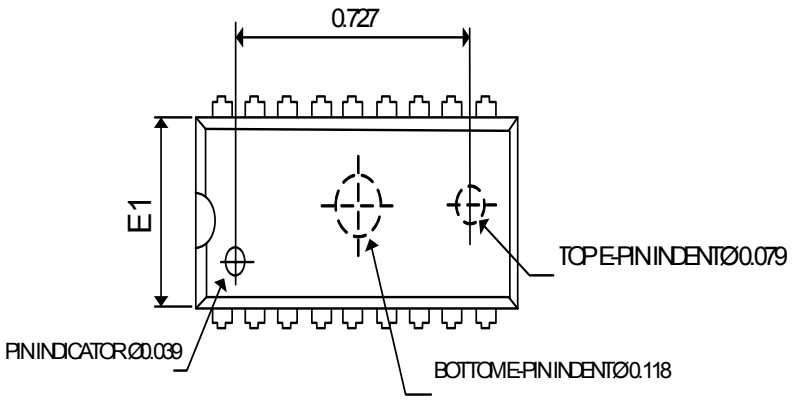
UNIT:INCH

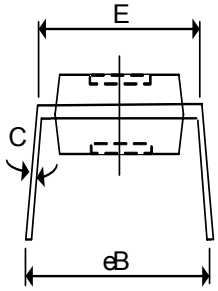
Note:

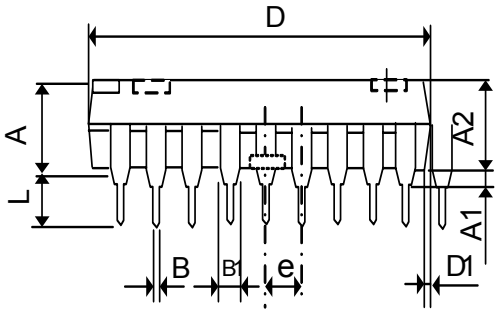
1.JEDEC OUTLINE:MS-013 AB
2.DIMENSIONS"D" DOES NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.MOLD FLASH,PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED.15mm(.006in) PER SIDE.
3.DIMENSIONS"E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS.INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED.25mm(.010in) PER SIDE.



18 PIN DIP

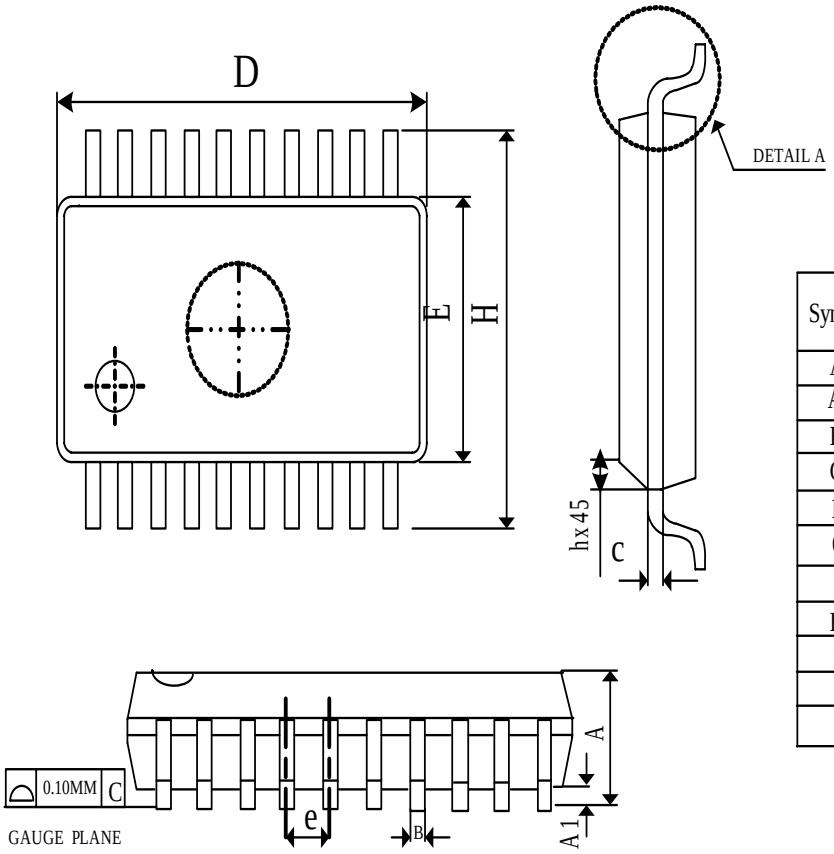






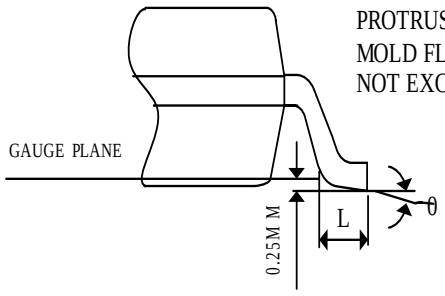
SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—		20		20	
A1	0.38	.100			2.54	
A2	—	3.30	3.56	—	0.130	0.140
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	1.27	0.25	0.33	0.008	0.010	
D	22.71	22.96	23.11	0.894	0.904	0.910
D1	0.43	0.56	0.69	0.017	0.022	0.027
E	7.62	—	8.26	0.300	—	0.325
E1	6.40	6.50	6.65	0.252	0.256	0.262
E	.008	.012	.015	0.20	0.29	0.38
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.38		9.65	0.330		0.380

20 PIN SOP

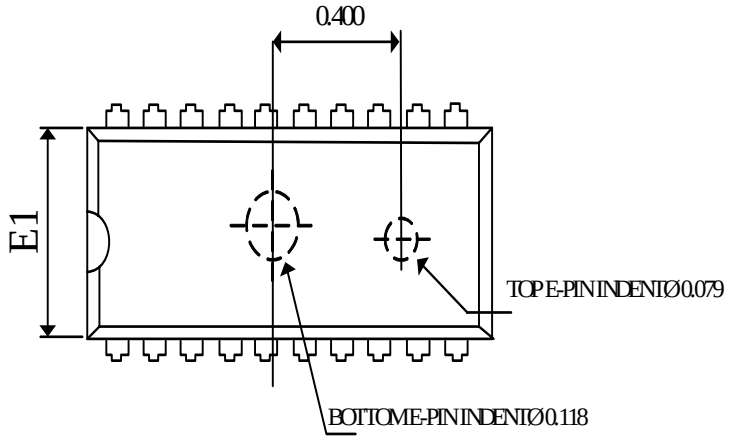


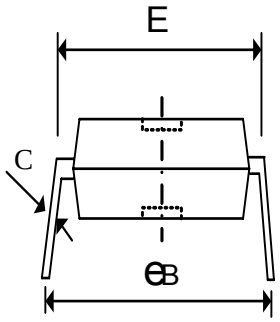
Symbol	DIMENSION IN MM		DIMENSION IN INCH	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.0091	0.0125
D	12.60	13.00	0.4961	0.5118
e	1.27 BSC		0.050 BSC	
E	7.40	7.60	0.2914	0.2992
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

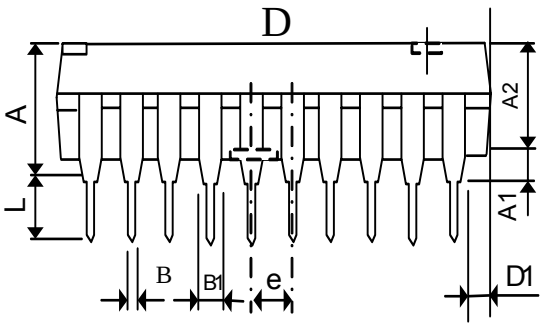
*Note:DIMENSION"D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH)PER SIDE.



20 PIN DIP

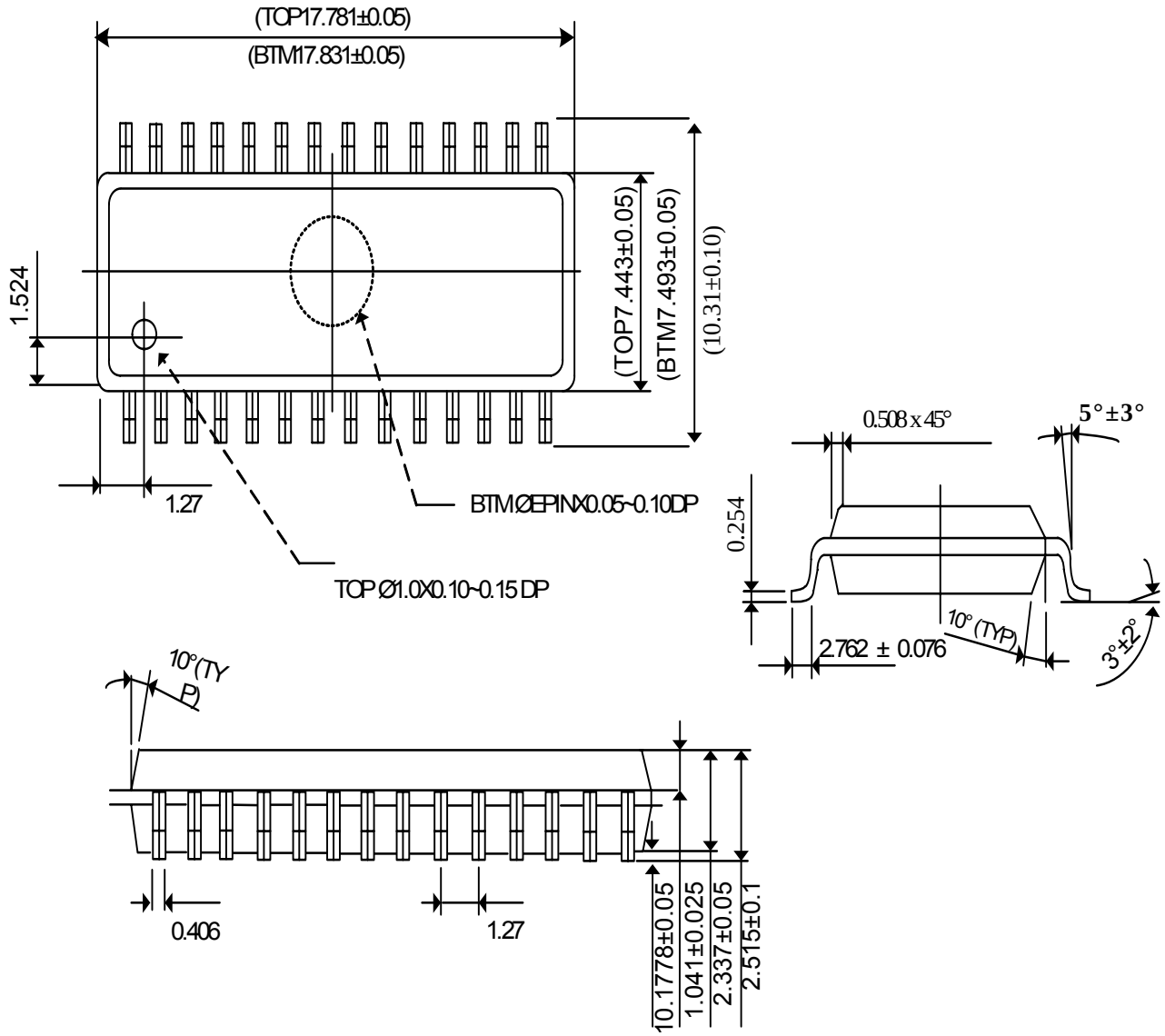




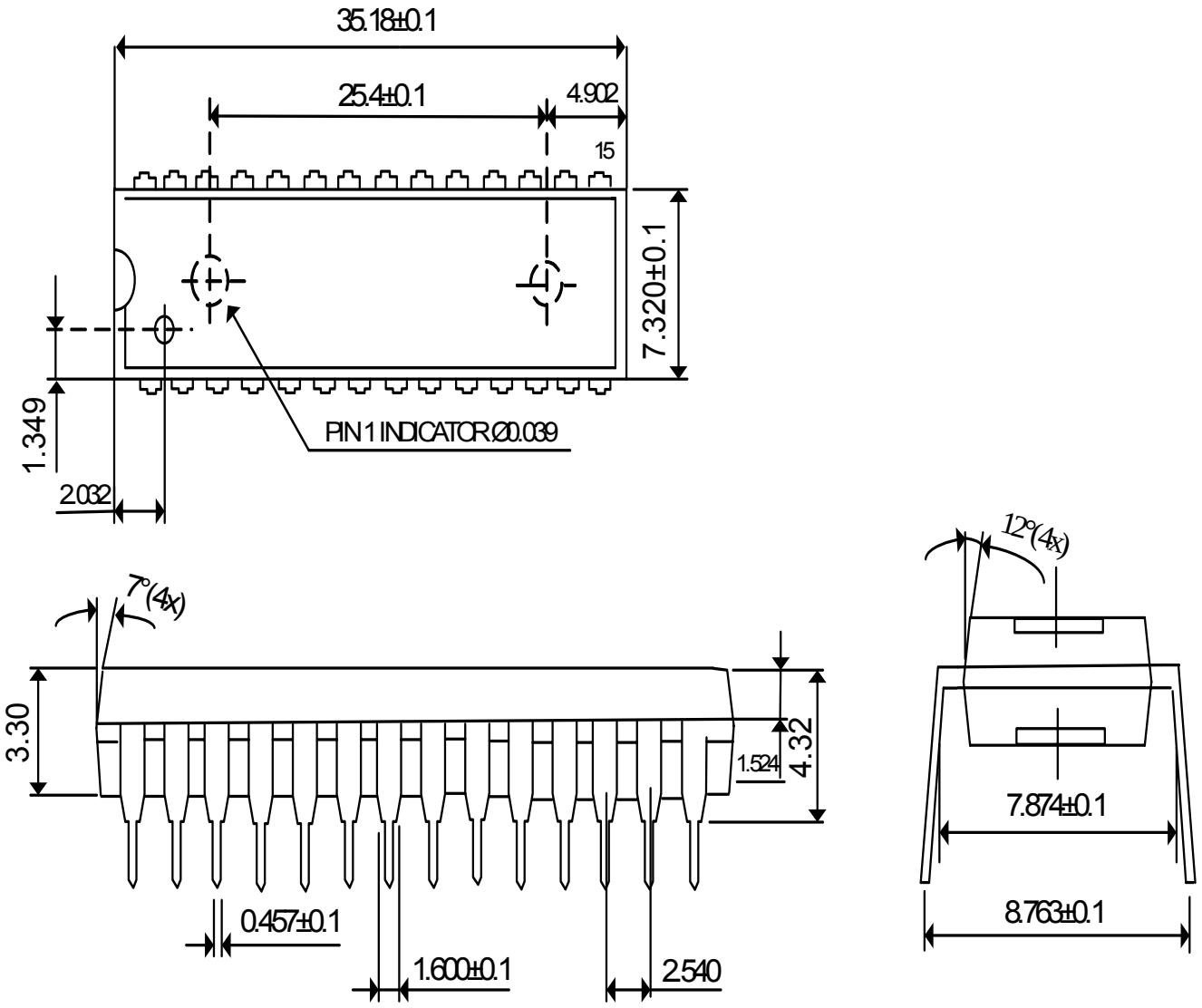


SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	4.57	—	—	0.180
A1	0.38	—	—	0.015	—	—
A2	—	3.30	3.56	—	0.130	0.140
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	26.32	26.416	26.52	1.036	1.040	1.044
D1	0.43	0.56	0.69	0.017	0.022	0.027
E	7.62	—	8.26	0.300	—	0.325
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	—	2.54	—	—	0.100	—
L	3.18	—	—	0.125	—	—
eB	8.38	—	9.65	0.330	—	0.380

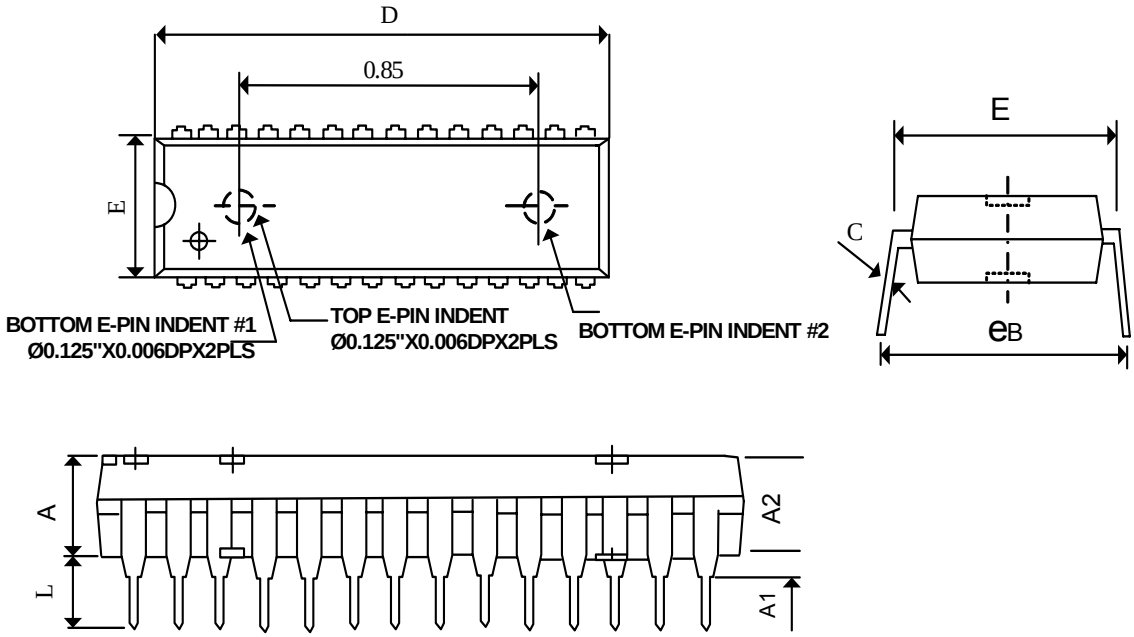
28 PIN SOP


(TOP17.781±0.05)
(BTM17.831±0.05)
(TOP7.443±0.05)
(BTM7.493±0.05)
(10.31±0.10)
1.524
1.27
BTMØ0EPINX0.05~0.10DP
TOP Ø1.0X0.10~0.15 DP
0.508 x 45°
5°±3°
0.254
2.762 ± 0.076
10° (TYP)
3°±2°
10°(TYP)
0.406
1.27
10.1778±0.05
1.041±0.025
2.337±0.05
2.515±0.1

28 PIN SKDIP


35.18±0.1
25.4±0.1
4.902
15
7.320±0.1
PIN 1 INDICATOR Ø0.039
1.349
2.032
7°(4x)
3.30
1.524
4.32
0.457±0.1
1.600±0.1
2.540
12°(4x)
7.874±0.1
8.763±0.1

28 PIN DIP



NOTES :

1. CONTROLLING DIMENSIDN : INCH
2. LEAD FRAME MATERIAL:ALOY 42
3. DIMENSION"D"AND "E1" DOES NOT NCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010"[0.25mm].
4. DIMESION"B1" DO NOT INCLUDE DAMBAR PROTRUSION.DAMBAR PROTRUSION SHALL NOT EXCEED 0.010"[0.25mm].
5. TOLERANCE :± 0.010" UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT:JEDEC SPEC MO-015-AH.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	5.59	---	---	0.220
A1	0.38	---	---	0.015	---	---
A2	3.71	3.91	4.11	0.146	0.154	0.162
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.33	0.008	0.010	0.013
D	36.58	37.14	37.34	1.440	1.462	1.470
D1	0.13	---	---	0.005	---	---
E	15.24	---	15.88	0.600	---	0.625
E1	13.64	13.89	14.15	0.537	0.547	0.557
e	---	2.54	---	---	0.100	---
L	3.18	---	4.06	0.125	---	0.160
eB	15.88	---	16.89	0.625	---	0.665